CLAIMS

1. An integrated circuit, comprising:

a first external pin; and

an input buffer connected to the first external pin, wherein the input buffer includes an output terminal and a first test mode input terminal adapted to disable the output terminal in response to a first test mode signal.

2. The integrated circuit of claim 1, the input buffer further including:

a disable input terminal adapted to disable the input buffer in response to a disable signal.

3. The integrated circuit of claim 1, wherein the input buffer provides a logic low output at the output terminal when the input buffer is disabled.

4. The integrated circuit of claim 1, wherein the input buffer provides a logic high output at the output terminal when the input buffer is disabled.

5. The integrated circuit of claim 1, further comprising:

a second external pin connected to the first test mode input terminal and adapted to receive the first test mode signal.

6. The integrated circuit of claim 1, further comprising:

a second external pin adapted to receive an external input signal;

a delay element connected to the second external pin adapted to provide a delayed input signal, wherein the delay element is connected to the first test mode input terminal.

7. The integrated circuit of claim 6, wherein the external input signal comprises an external clock signal.

8. The integrated circuit of claim 1, wherein the input buffer includes:

a first transistor connected to a voltage source, the gate input of the first transistor being connected to the first test mode input terminal;

a second transistor connected to the first transistor and the output terminal, the gate input of the second transistor being connected to the input terminal;

a third transistor connected to the output terminal and ground, the gate input of the third transistor being connected to the input terminal; and

a fourth transistor connected between the output terminal and ground, the gate input of the fourth transistor being connected to a second test mode input terminal.

9. The integrated circuit of claim 8, wherein the fourth transistor grounds the output terminal of the input buffer in response to the second test mode signal.

10. The integrated circuit of claim 8, wherein the first transistor isolates the second transistor from the voltage source in response to the first test mode signal.

11. The integrated circuit of claim 8, wherein the first and second transistors comprise p-channel transistors and the third and fourth transistors comprise n-channel transistors.

12. The integrated circuit of claim 1, wherein the input buffer includes:

a first transistor connected to ground, the gate input of the first transistor being connected to a second test mode input terminal;

a second transistor connected to the first transistor and the output terminal, the gate input of the second transistor being connected to the input terminal;

a third transistor connected to the output terminal and a voltage source, the gate input of the third transistor being connected to the input terminal; and

a fourth transistor connected between the output terminal and a voltage source, the gate input of the fourth transistor being connected to the first test mode input terminal.

13. The integrated circuit of claim 12, wherein the fourth transistor connects the output terminal of the input buffer to the voltage source in response to the first test mode signal.

14. The integrated circuit of claim 12, wherein the first transistor isolates the second transistor from ground in response to the second test mode signal.

15. The integrated circuit of claim 12, wherein the first and second transistors comprise n-channel transistors and the third and fourth transistors comprise p-channel transistors.

16. The integrated circuit of claim 1, wherein the first test mode input terminal is adapted to drive the output terminal to a first logic state in response to the first test mode signal, and wherein the input buffer includes a second test mode input terminal adapted to drive the output terminal to a second logic state in response to a second test mode signal.

17. The integrated circuit of claim 1, wherein the input buffer further includes:

a second test mode input terminal adapted to disable the input buffer in response to a second test mode signal.

18. The integrated circuit of claim 17, further comprising:

a second external pin connected to the second test mode input terminal and adapted to receive the second test mode signal.

19. The integrated circuit of claim 17, further comprising;

a second external pin adapted to receive an external input signal; and

a delay element connected to the second external pin adapted to provide a delayed input signal, wherein the delay element is connected to the second test mode input terminal.

20. The integrated circuit of claim 8, wherein the input buffer includes:

a second test mode input terminal adapted to receive a second test mode signal;

a fifth transistor connected between the third transistor and ground, the gate input of the fifth transistor being connected to the first test mode input terminal;

a sixth transistor connected between the output terminal and a voltage source, the gate input of the sixth transistor being connected to the second test mode input terminal.

21. The integrated circuit of claim 20, wherein the fifth transistor isolates the second transistor from ground in response to the first test mode signal.

22. The integrated circuit of claim 20, wherein the sixth transistor connects the output terminal of the input buffer to the voltage source in response to the second test mode signal.

23. The integrated circuit of claim 20, wherein the fifth transistor comprises an n-channel transistor and the sixth transistor comprises a p-channel transistor.

24. A method for testing an integrated circuit, the integrated circuit including a first external pin and an input buffer, the method comprising:

providing a first external input signal to the first external pin at a first specified time;

disabling the input buffer at a second specified time after the first specified time.

25. The method of claim 24, further comprising:

providing a clock signal to the integrated circuit, the clock signal including an edge defined by a transition in the clock signal between first and second logic states, wherein the first specified time comprises a first specified time interval before the edge and the second specified time comprises a second specified time interval after the edge.

26. The method of claim 24, the integrated circuit including a second external pin, the method further comprising:

providing a second external input signal to the second external pin, wherein the disabling comprises disabling the input buffer in response to the second external input signal.

27. The method of claim 24, the integrated circuit including a second external pin, the method further comprising:

providing a second external input signal to the second external pin,

delaying the second external input signal to generate a delayed input signal, wherein the disabling comprises disabling the input buffer in response to the delayed input signal.

28. The method of claim 24, the input buffer including an output terminal, wherein the disabling comprises grounding the output terminal.

29. The method of claim 24, the input buffer including an output terminal, wherein the disabling comprises connecting the output terminal to a voltage source.

30. The method of claim 24, the input buffer including an output terminal, further comprising:

providing a first test mode signal; and

providing a second test mode signal,

wherein the disabling comprises disabling the output terminal to a first logic state in response to the first test mode signal and disabling the output terminal to a second logic state in response to the second test mode signal.

31. An integrated circuit, comprising:

a first external pin; and

an input buffer connected to the first external pin, wherein the input buffer includes an output terminal and first and second test mode input terminals, the first and second test mode input terminals adapted to disable the output terminal in response to respective first and second test mode signals;

a second external pin adapted to receive an external clock signal; and

a delay element connected to the second external pin and adapted to provide a delayed clock signal, the delay element being coupled to the second test mode input terminal.

32. The integrated circuit of claim 31, the input buffer further including:

a disable input terminal adapted to disable the input buffer in response to a disable signal.

33. The integrated circuit of claim 31, wherein the input buffer provides a logic low output at the output terminal in response to the input buffer being disabled.

34. The integrated circuit of claim 31, wherein the input buffer provides a logic high output at the output terminal in response to the input buffer being disabled.

35. The integrated circuit of claim 31, wherein the input buffer includes:

a first transistor connected to a voltage source, the gate input of the first transistor being connected to the first test mode input terminal;

a second transistor connected to the first transistor and the output terminal, the gate input of the second transistor being connected to the input terminal;

a third transistor connected to the output terminal and ground, the gate input of the third transistor being connected to the input terminal; and

a fourth transistor connected between the output terminal and ground, the gate input of the fourth transistor being connected to the second test mode input terminal.

36. The integrated circuit of claim 35, wherein the fourth transistor connecting the output terminal of the input buffer to the voltage source in response to the second test mode signal.

37. The integrated circuit of claim 35, wherein the first transistor isolates the second transistor from the voltage source in response to the first test mode signal.

38. The integrated circuit of claim 35, wherein the first and second transistors comprise p-channel transistors and the third and fourth transistors comprise n-channel transistors.

39. The integrated circuit of claim 31, further comprising:

an inverter having an input connected to the delay element and an output connected to the first test mode input terminal.